

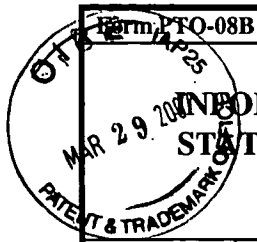
Form PTO-08A <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>				<i>Complete if Known</i>	
				Application Number	10/593,807
				Filing Date	9/21/06
				First Named Inventor	Turner, Steven E.
				Group Art Unit	
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	20040084 US

[illegible][illegible]

Examiner Signature		Date Considered	
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\* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /TM/



Form PTO-08B				Complete if Known	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>				Application Number	10/593,807
				Filing Date	9/21/06
				First Named Inventor	Turner, Steven E.
				Group Art Unit	
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	20040084 US

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No.	(Including Name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc...), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	T	
		TURNER, ET AL., Benchmark Results For High-Speed 4-Bit Accumulators Implemented In Indium Phosphide DHBT Technology, IEEE Lester Eastman Conference on High Performance Devices, Rensselaer Polytechnic Institute, August 4-6, 2004		
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		MATHEW, ET AL., 2-Bit Adder Carry and Sum Logic Circuits Clocking at 19 GHz Clock Frequency in Transferred Substrate HBT Technology, Dept of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, GTRAN Inc, Newbury Park, CA 91320		
		DVORAK, ET AL., 300 GHz InP/GaAsSb/InP Double HBTs with High Current Capability and $BV_{CEO} \geq 6V$ , IEEE Electron Device Letters, Vol. 22, No. 8, August 2001, pp 361-363		
		SALOUS, ET AL., FPGA-based Hybrid Accumulator Architecture for Digital Chirp Synthesis, Int. J. Electronics, 1996, Vol. 80, No. 3, pp 441-447		
		BETOWSKI, ET AL., Considerations for Phase Accumulator Design for Direct Digital Frequency Synthesizers, School of Electrical Engineering & Computer Science, Washington State University, Pullman, WA 99164		
		MATHEW, ET AL., 2-Bit adder: Carry and Sum Logic Circuits at 19 GHz clock frequency in InAlAs/InGaAs HBT Technology, Electronics Letters, Vol. 37, No. 19, September 13, 2001, pp 1156-1157		

Examiner Signature	/Tan Mai/	Date Considered	09/24/2008
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